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Ex. 3.4 Solution: Modern Processor Design by John Paul Shen and Mikko H. Lipasti : Solution Manual Q.3.4: Consider a cache with 256 bytes. Word size is 4 bytes and block size is 16 bytes.

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Ex 4.8 Solution : Modern Processor Design by John Paul Shen and Mikko H. Lipasti : Solution manual Q.4.8: In an in-order pipelined processor, pipeline latches are used to hold result operands from the time an execution unit computes them until they are written back to the register file during the writeback stage.

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Ex 2.16 & 2.17 Solution: Modern Processor Design by John Paul Shen and Mikko H. Lipasti : Solution Manual : Q.2.16: In a TYP-based pipeline design with a data cache, load instructions check the tag array for a cache hit in parallel with accessing the data array to read the corresponding memory location.

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Ex. 3.1 & 3.3 Solution: Modern Processor Design by John Paul Shen and Mikko H. Lipasti : Solution Manual Q.3.1: Given the following benchmark code, and assuming a virtually-addressed fully-associative cache with infinite capacity and 64 byte blocks, compute the overall miss rate (number of misses divided by number of references).

Ex. 3.1 & 3.3 Solution: Modern Processor Design by John ...

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